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Digital IF Design

In response to the pressures for multi-band, multi-mode cellular handset operation, digitally sampled receiver IF implementations are becoming the norm. The high performance obtainable through these techniques will also provide the solution to 3G (WCDMA/cdma2000) requirements.

IF sampling is achieved by presenting the downconverted RF – usually after anti-alias filtering with the bandwidth of a single modulated channel – to a high performance sampling analogue-to-digital converter, a sampling ADC. In the case of base station designs multiple channels are frequently sampled in a wide band process with channel tuning/selection being performed digitally.

The sampling ADC comprises a sample-and-hold (S/H) function and an analogue to digital converter. The S/H is responsible for sampling the incoming analogue waveform and holding the sample while the digital conversion takes place. The ADC part performs the conversion process. The two functions together may also be referred to as a digitiser.

Sitting at the interface between the analogue IF signal and the digital signal processor (DSP) the ADC performance must be qualified in terms of both its analogue sampling capability and its digital conversion capability. This application requires a focus on some of the less traditional performance parameters of the ADC. A few definitions and examples of the effects of the relevant parameter performance will highlight areas of importance.

The dynamic range of a typical mobile wireless terminal is in excess of 100 dB. To digitise this order of dynamic range would require a converter in excess of 18 bits. Given the power and cost restrictions of handset implementation this complexity is unacceptable. To address this problem the dynamic range is reduced prior to conversion by means of a variable gain amplifier (VGA) employed in an automatic gain control system (AGC). In this way the conversion process can be achieved using an 8 or 10 bit converter. In the case of the very large post conversion processing gains (eg 30 dB) available in wide band CDMA systems resolution maybe reduced to 6 or even 4 bits.

The sampling ADC may be characterised by parameters more relevant to the digital receiver application.

The **Signal-to-Noise Ratio (SNR)** of the Sample and Hold (S/H) and ADC together is the ratio of the full scale analogue input (rms) to the wideband noise (rms). Wideband noise includes quantization error and any other non-harmonic spurious or background noise. It is generally specified at specific input frequencies and sampling rates.

Signal-to-(Noise + Distortion) (SINAD) is defined as the previous SNR but includes generated harmonic components.

For both SNR and SINAD, noise is the rms sum of the spectral components below the Nyquist frequency and excludes DC.

In the case of a perfect or 'ideal' ADC the only noise would be due to quantization. Quantization is the difference between the digitally representative output and the analogue input. It has the classic staircase construction where each 'tread' represents 1 Least Significant Bit. Thus any analogue input level can have uncertainty of ± 0.5 LSB. Given the rms summation of the error, the SNR of the 'ideal' converter has a value of 6.02n + 1.76 dB where n equals the number of bits.

It follows that the ideal SNR can be tabulated against n

n	**'Ideal' SNR dB**
4	25.84
6	37.88
8	49.92
10	61.96
12	74.00
14	86.04

Table 1

An often applied rule of thumb for a realisable SNR is to multiply the resolution by six, eg 6 bit converter SNR = 36 dB. This rule should not be applied for converters above 12 bits as different noise mechanisms dominate, eg flicker noise.

Although not telling the whole story the SNR does indicate how closely the practical noise performance reaches to the 'ideal' performance.

The SINAD performance tells more of the story in a typical signal sampling application. As it includes both noise and discrete spurii it quantifies all signal products that appear in the converted output.

The harmonic part of the SINAD expression can also be dimensioned separately as **Total Harmonic Distortion (THD)**. This is the rms sum of all the harmonics in the output signal bandwidth of interest. In practice only the first three or five are considered, as these represent most of the harmonic distortion present. By careful selection of the sampling rate and IFs the impact of harmonic distortion in a digital receiver can be minimised.

An overall assessment of the sampling converter can be expressed in terms of the **Effective Number of Bits (ENOB)**. It is derived from the SINAD expression and includes not only (quantization + wideband) noise and harmonics but also missing codes, AC/DC non-linearities and phase or aperture jitters

ENOB is usually shown as

$$\frac{SINAD\,(dB) - 1.76}{6.02}$$

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ENOB is also seen with SNR substituted for SINAD but is a less ‘all-encompassing’ definition.

More correctly a second term should be added to this formula

[20log(full scale amplitude/actual input amplitude)]/6.02.

This term shows ENOB increasing with decreasing input amplitude although it is a less significant factor, unless the input is considerably below full scale.

Of considerable importance in IF sampling applications is **Spurious Free Dynamic Range (SFDR)**. This parameter characterises the converters in band harmonic performance. It is the ratio of the rms value of the fundamental signal to the rms value of the largest distortion component. Although this is usually assumed to be a harmonic of the fundamental other large spurii may be observed, e.g. the converter clock may couple into circuit due to poor layout, ineffective isolation or cross talk. SFDR is another qualification of the non-linearity of the ADC processes and is important, as it may be the limiting factor of the receiver's dynamic range. In this way signals of interest may not be recovered or spurs may appear to be adjacent channel signals.

As SFDR is a prime system performance determining parameter the designer may make the decision to trade a lower SNR for an improved SFDR. This dynamic range improvement can be obtained by restricting the full scale input range. The designer must ensure that the SFDR figure obtained before the trade off adjustment is due to conversion non-linearities and not ‘pick up’ spurii. The latter would be unaffected by a reduction in input range.

A second method to trade SNR against SFDR is by the inclusion of dither, this is achieved by adding an out-of-band noise signal.

Although the amount of dither required is ADC specific the technique applies to all converters. The inclusion of dither randomises the coherent spur energy that occurs in the ADC. Although the level of spur energy is unaltered it is transformed (spread) into a small increase of floor noise level over the entire ADC bandwidth. Indeed, the addition of dither helps to distinguish those spurs that are caused by ADC non-linearities and those that are externally generated.

Static Noise is another parameter that is frequently seen as a measure of ADC performance. Static noise relates to the bit variation that occurs with a fixed DC input. This would normally be expected to change by no more than 1 LSB. High speed converters can have static noise figures of 5 or even 7 dB. This parameter is rarely of concern in wireless sampling applications as DC signals are infrequently processed. However, to prevent this parameter reducing dynamic range it is recommended that

the ADC input is AC coupled and not externally biased up to mid-rail in the usual way.

SAMPLE AND HOLD FUNCTION

Although the SINAD, ENOB and SFDR characterisations include noise and distortion mechanisms that occur in both the S/H and conversion section, it is valuable to consider the requirements of the S/H section independently.

Aperture Jitter – a_j – results from noise that is superimposed on the 'Hold' command; ie it affects its timing. It is specified as an rms value.

A 'rule of thumb' may be applied to this parameter –i.e. the signal must not change by more than ± ½ LSB during the aperture jitter time. Using a Full Scale Sinewave V = sin(2p ft) then

$$\frac{dV}{dt} = 2\pi fA\cos(2\pi ft) < \frac{\pm\frac{1}{2}LSB}{ta_j}$$

$$As\ \frac{1}{2}LSB = \frac{A}{2^n}\ where\ n = no\ of\ bits$$

$$\therefore f < \frac{1}{2\pi \times 2^n \times ta_j}$$

Eg A 10 bit ADC with a S/H aperture jitter of 10 ps.

therefore *f*max = 15.54 MHz

Note ADC sampling rate must be at least 2 X 15.54 MHz.

Table 2 shows the frequency (f MHz) capability for a range of aperture jitters by ADC resolution.

Aperture	**ADC Resolution**			
Jitter a_j (ps)	**6**	**8**	**10**	**12**
1	2487	621	155	38
2	1243	310	77	19
5	497	124	31	7.6
10	248	62	15	3.8
20	124	31	7.7	1.9
50	49	12	3.1	0.76
100	24	6	1.5	0.38

Table 2

Note The Nyquist criterion requires that the ADC sampling rate be at least twice the

frequency shown in Table 2.

SUMMARY

The sensitivity and selectivity of the superhet receiver in both analogue and digital applications is primarily determined by the front end (filter, LNA, mixer, and LO purity) performance and to a lesser degree the IF and demodulator performance.

The IF and demodulator sections have traditionally achieved their performance through the use of highly specified filters, resonators, mixers and amplifiers. A consequence this approach however, has been the inflexibility of the specification; it has not been possible to perform adaptive signal management or to 'fine-tune' the receiver in its application. A second concern is the degree of testing/adjustment that the traditional component line up requires.

The adoption of analogue IF to digital conversion and the subsequent signal processing capabilities are reducing this inflexibility and also reducing test complexities in these areas.

Of course, it is important to ensure the overall receiver specification is not degraded, (indeed, improved performance is expected with each new generation) by the increasing degree of digital processing.

It is the parameters defined above that are taking the place of the more traditional considerations of insertion loss, group delay and stability as well as cost, weight and size in the mobile phone handset.

On analysing the performance requirements of third generation, wideband CDMA phone technology, the inescapable conclusion is reached that only by the careful application of such digital technologies will handset/terminal realisation be possible.

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