# RTT TECHNOLOGY TOPIC
# November 1999

## WCDMA Processing Gain

In the October Hot Topic (3G Demodulation Budget) a required Carrier-to-Noise Ratio (CNR) figure was derived based on the modulation format, the demodulator characteristic, the bit rate and the required quality of output for the digital receiver process.

The example chosen used QPSK modulation as this is to be used for W-CDMA. It was found that using QPSK modulation with a specified output quality (BER) of 1 x $10^{-3}$, a CNR of 6.8 dB was required, and for a BER of 1 x $10^{-6}$ a CNR of 10.5 dB was needed. These figures were derived before the benefits of coding gain were added.

This CNR is the necessary quality of signal required at the input to the demodulation process, ie the signal supplied by the IF output. These figures are valid regardless of the method of demodulator implementation, eg hardware or software.

If a digitally processed software (or dedicated digital hardware) demodulation method is used, the IF presented to the demodulator will be in the form of a digitised IF signal. The analogue IF to digital IF conversion is performed by a sampling analogue to digital converter (ADC). The necessary characteristics of this component were explored in the June 99 Hot Topic.

In wireless systems using non-spread spectrum techniques it is important to evaluate the ADC noise and distortion contribution and to ensure that these distortions are negligible, hence have little or no effect, on the CNR of the signal passing through the analogue to digital conversion process. This need to preserve signal quality is one of the prime parameters determining the ADC performance, particularly the number of bits (resolution).

If a direct sequence spread spectrum process is considered a different situation is seen. A fundamental principle of the spread spectrum process is that prior to the baseband processing an improvement in CNR can be obtained.

The commercial application of the Spread Spectrum process uses direct sequence spread spectrum (DSSS). In this system the randomised data (digital) to be transmitted is multiplied (exclusive-ored) by a pseudo random (PN) binary sequence. The PN code is at a much higher rate than the data and so the resultant occupied bandwidth is defined by the PN code rate. The PN rate is referred to as the chip rate with the PN symbols as chips.

The resultant ‘wideband’ signal is transmitted and hence received by the spread spectrum receiver. In the receiver this wideband signal is multiplied by the same PN sequence that was used in the transmitter to spread it. For the process to recover the original pre-spread signal energy it is necessary that the de-spreading multiplication

takes place synchronously with the incoming signal.

A key advantage of this process is in the way in which interference signals which are encountered in the propagation channel are processed. As the received signal multiplication (de-spreading) is synchronous to the received signal the original narrow band signal energy is recovered. However, any interfering signals received are also multiplied by the receiver PN sequence **but not synchronously**. Thus the interfering signals are spread over the wide band width with only a small amount of interfering energy falling in the recovered narrow band signal.

The processing (or de-spreading) gain experienced in the DSSS process is the ratio of the chip rate to the data rate.

**Example:**

If a 32 kb/s data rate is spread with a chip rate of 3.686 Mchips/s then the processing gain is

$$\frac{3.686E6}{32E3} = 115$$

$$= 20.6dB$$

The power of this process can be seen by reference to the CNR in the receiver IF/Demodulator.

EG: It was seen in the October Hot Topic that a CNR of 6.8 dB was required for 1 x $10^{-3}$ BER and 10.5 dB for 1 x $10^{-6}$. If a data rate of 1024 kb/s is transmitted with a BER requirement of 1 x $10^{-6}$ then the processing gain is 5.5 dB. If the signal quality, ie CNR is improved by 5.5 dB and a CNR of 10.5 dB is required at the demodulator input then the receiver will still achieve the desired performance with a CNR of 5.0 dB in the IF/RF stages.

Back to the IF analogue to digital conversion. The processing gain is applied after the IF digitisation process. This means the ADC is working in the ‘low quality’ (5.0 dB CNR) signal environment and as such the number of bits required can be reduced in accordance with the definitions presented in the June 99 Hot Topic – Digital IF Design.

It must be recognised that the process gain is a function of the total spread content of the channel.

The total spread content of the channel is formed by a Dedicated Physical Data Channel (DPDCH) being multiplexed together with a Dedicated Physical Control Channel (DPCCH). These are multiplexed across 16 time slots, each of 0.625 ms to make up a 10 ms frame.

An example:

A DPDCH is constructed of

- Source coded content, eg = 9.6 kb/s.
- This is then channel coded (9.6 kb/s x 3) = 28.8 kb/s. (Channel coding is the process of encoding the source data to increase its robustness, in this example convolutional encoding at a 1/3 rate).
- Now the DPCCH is added in – each frame (10 ms) contains 160 control symbols, ie 10 symbols per slot.

160 symbols/10 mS = 1600 symbols/sec.

As the baseband data is formatted in QPSK then 1600 sym/sec = 3.2 kb/s.

So the slot total is = 28.8 + 3.2 kb/sec

= 32 kbs

= 16 k symb/sec

The signal is then QPSK modulated and spread using a cover of 240 chips/symbol.

240 x 16 = 3.84 Mc/s

Prior to the recent change to 3.84 Mc/s the chip rate was at 4.096 Mc/s, which when applied to a filter with a roll of factor (μ ) of 1.22 gave a bandwidth of 5 MHz.

The change to 3.84 Mc/s would assume a filter roll off factor of 1.47 30 giving the possibility of an improved adjacent RF ‘channel’ performance.

As the channel code rate is 32 kbs the process gain is 10 log (3.84/0.032) = 20.8 dB, not 10log (3.84/0.0096) = 26 dB as may have been anticipated (or hoped for!).

In addition to the process (de-spreading) gain described there is the received signal power improvement due to multipath reception and combining them.

The quality of this process depends on the ability of the receiver to accurately estimate the various multipath delays at a sufficient rate and to combine the recovered energies with a minimum of loss.

It is necessary to have at least one chip ‘distance’ between multipaths to be able to resolve then separately and hence use their energy. It follows therefore that the shift from a chip rate of 4.096 Mcs to 3.84 Mcs has diminished the improvement that the RAKE receiver can offer, but not to a significant degree, ie

| | |
|---|---|
| 4.096 Mc/s | = 0.2441 m S |
| Path length for 1 chip | = 73.23 m |
| 3.84 Mc/s | = 0.264 m S |

| | |
|---|---|
| | = 78.12 m |
| Path difference | » 5 m |

When used in picocells or small microcells, path lengths of these orders may not be obtained and hence RAKE gain will not be realized. In larger cells the number of paths processed by the RAKE receiver depends primarily on the amount of processing power that the designer is prepared to devote to the task and the losses in the RAKE combine process. Typically four or five RAKE fingers are anticipated using a dynamic allocation process to keep them to the strongest paths but also allocate them as required to pilot channel resolution.

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