RTT TECHNOLOGY TOPIC
December 1999

3G DSP

The Story So Far

The June 99 Hot Topic – 'Digital IF Design' – defined some of the sampling analogue-to-digital converter (ADC) parameters of importance in wireless signal conversion applications. It also reviewed the signal environment in which this important component is placed and quantified parameters that have a direct influence on the wireless performance.

The consideration of the wireless system performance was continued in the September 99 Hot Topic – '3G Receiver Noise Budget'. This analysis reviewed the principles of Direct Sequence Spread Spectrum as applied to CDMA and took as a start point a typical W-CDMA system BER, Modulation type, Bandwidth, Spreading rate and data rate requirement.

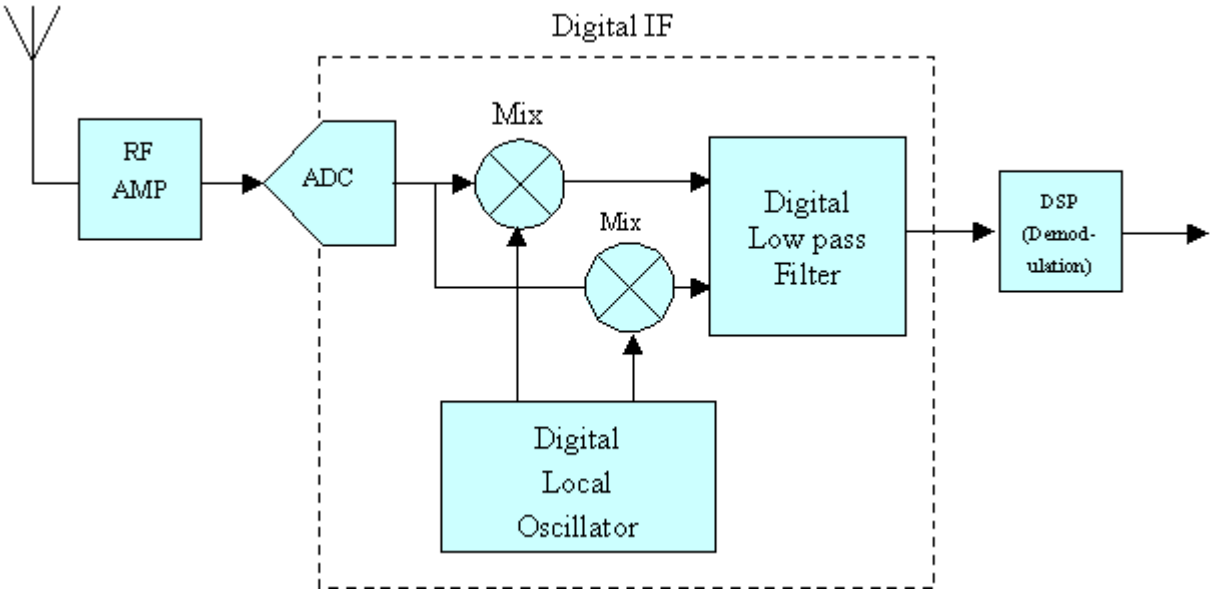
The analysis derived the bandwidth of the system, given the modulation type and from this derived a noise floor performance for an ideal receiver.

The October 99 Hot Topic – '3G Demodulation Budget' – continued the analysis. Using the specified output BER requirement and the modulation type (QPSK) the performance of the demodulation process was defined in terms of it's E_b/N_o. Applying the bandwidth and bit rate gave the Carrier-to-Noise ratio (CNR) required at the input to the demodulator. This CNR was played into the figures produced in the September Hot Topic to produce receiver sensitivity figures. The contribution of coding gain to sensitivity was also considered.

The November 99 Hot Topic 'W-CDMA Processing Gain' defined processing gain and gave an example of the relaxation that is possible (given sufficient processing gain) in the required CNR through the IF stages. This in turn allowed the sampling ADC resolution to be reduced to 6 or even 4 bits. The application of the processing gain was considered by both total channel throughput and by message traffic throughput.

The Story Moves On:

THE DIGITAL RECEIVER



So far these topics have addressed the signal processing parameters principally in terms of ADC and demodulator performance. However, if improved performance, ie sensitivity, selectivity, cost, is to be achieved, the RF and IF processing before analogue to digital conversion must be considered in detail. Equally, the processing after signal conversion must be considered in detail if 'best performance' is to be obtained.

In traditional analogue design the gain/noise budget has had the objective of presenting a good quality CNR signal to the demodulator.

The digital IF process puts an ADC in the IF strip. This now creates a new set of criteria to meet for the designer.

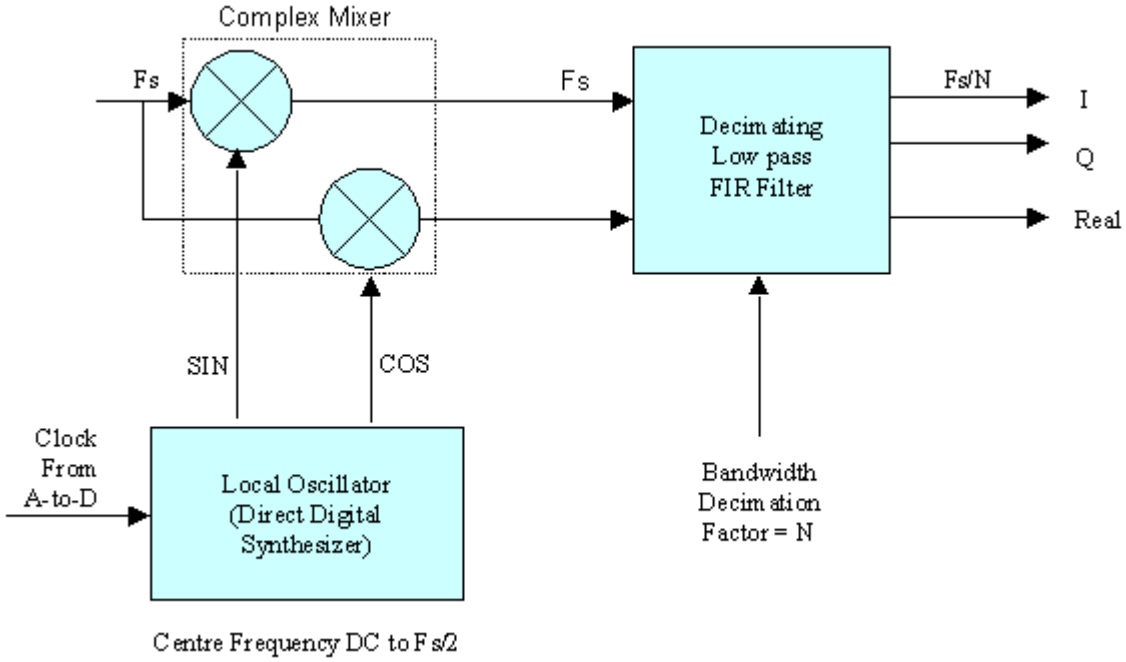
Any ADC has a minimum quantization level, ie the smallest level signal that can be 'seen' by the ADC, the minimum input signal must reach at least this level in order to be converted. The approach is to ensure that the noise floor of the Signal-to-Noise Ratio (SNR) input signal reaches at least this level. If the noise 'dithers' across a quantizing level then the benefits of an improved Spurious Free Dynamic Range (SFDR), as discussed in the June Hot Topic will be obtained.

So, the gap between the downconverted (IF) signal SNR and the minimum quantization level can be used to define the IF gain required prior to digital conversion. If this simple approach is taken it has the disadvantage of increasing the in band noise level. An alternative approach is to inject out-of-band noise into the signal path to raise the level of the signal. The out-of-band noise can be recognised as such by the DSP function after digitisation and so ignored or removed from the signal. In this way the quality of the in-band (on channel) signal is preserved.

The design approach to achieve this must be carefully considered and must be tailored to suit the particular ADC and levels in question.

After digitisation the samples must be processed to obtain the original baseband data.

THE DIGITAL IF



The samples are passed to a pair of digital mixers or multipliers where they are multiplied by the output from a digital oscillator. The digital oscillator generates precise [eg 32 bits precision (or greater)] digital value samples of both a sine and cosine wave. As the oscillator is clocked with the same clock (Fs) as the ADC the sine/cosine samples are generated at the same time as the A to D sample conversion takes place.

The effect of multiplying the two information sets (RF and LO) together is to shift the complete Fs/2 to Fs band in frequency. By varying the LO frequency around 0 Hz any narrowband (or wideband) part of the down converted spectrum may be placed at 0 Hz. The waveform must be processed in terms of its I and Q components in order to maintain the integrity of both the 'positive' and 'negative' frequencies.

The down converted I and Q samples are still at the ADC sample rate. The signal must now be processed to extract the modulation bandwidth. This filtering function is referred to as decimation and is the application of a finite impulse response (FIR) filter to the signal samples to reduce the bandwidth. As there is a bandwidth reduction there is a reduction in noise energy content and a consequent improvement in SNR. The low pass filter action is at a reduced frequency and so the decimation rate can be performed at a Nyquist frequency related to the filter bandwidth.

The output from this process may be taken as either a complex I and Q signal or as a 'real' signal.

Choices of ADC sampling frequency, ie Nyquist band positioning must be carefully considered in order to minimise the effects of aliased in-band products produced by

inevitable non-linearities in all parts of the system.

Also, the generation of AGC and AFC feedback information is a considerable design challenge given the wide dynamic range of data processed in modern wireless communications.

There are basically two design jobs to do in wireless – design a base station transceiver and design a handset (terminal or wireless appliance). In the past, these two design jobs have often been regarded as separate tasks with little or no commonality.

This is changing for three reasons – firstly, base stations are becoming smaller with lower power output, secondly there is a need to reduce costs – common silicon across the base station and handset would help and thirdly, handsets are having to support highly variable data rates – something which only base stations have had to process in the past.

The design and technology approach used in base stations is only prevented from being adopted in handsets by the DC power consumption. However, as the efficiency of semiconductor processes and integration scales improve, the reducing power consumption of previous 'base station only' techniques make these solutions viable for the handset.

Digitally sampled IFs were first seen in base station applications, where the approach was to use a conventional RF front end with the necessary system bandwidth, eg 25 MHz, followed by the traditional IF approach of filtering the bandwidth with analogue filters (SAW or ceramic) down to a single modulation bandwidth channel, eg GSM 200 kHz. This single narrow bandwidth channel could then be digitised with an ADC at typically ten or twenty million samples per sec (Msps). As the channel carried only one signal, automatic gain control (AGC) could be applied in order to reduce the dynamic range of the signal and so reduce the resolution requirement of the ADC from 16 or 18 to 8 or 10 bits.

While this approach was being engineered into base stations the handset was still using a traditional hardware IF and demodulator process. The only application of ADCs in the handset came after demodulation at baseband frequencies.

Base station design is now adopting a wide band approach where the RF front end is still of system bandwidth but the output of the down converting mixer is also full bandwidth. This full system bandwidth is then applied to a very high performance ADC. The whole digitised bandwidth is then presented to a powerful DSP (or part FPGA) in order to tune/filter individual channels as well as demodulate, de-interleave and decode the data.

As multiple channels are processed simultaneously it is not possible to generate an AGC function as in the single system, as weak signals may be lost if the gain is reduced. This minimisation (or removal) of the AGC also means that strong signals are less attenuated, ie the RF section and ADC require a larger dynamic range. The receiver front end must be designed with considerably greater 'head room' (but not at the sacrifice of sensitivity) and the ADC must have a larger number of bits and

sample at a faster rate. Example performance requirements might be 1 GHz input sampling capability, 65 Msps sampling rate and a 14 bit resolution.

While this exciting level of performance is being engineered into base stations, the handset is now being designed with sampling IFs processing a single channel, ie handset development follows on the heels of base station.

In order to achieve optimum performance from both base stations and handsets a high degree of attention must be paid to each individual step of the processing as well as a total system consideration.

To increase the commonality of design approach between handset and base station, similar architectures and indeed identical hardware may be used by adopting the technique of running a particular DSP at 3 or 5 volts when used in the base station and using the same device in the handset powered at 1v. Lucent's DSP 16000 is one example of this doubling as a base station DSP running at 3 volts and a 1 volt handset DSP (running at a lower clock rate).

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