# RTT TECHNOLOGY TOPIC
# July 2003

## The impact of the traffic mix shift on network hardware (2)

In our June HOT TOPIC we argued that as session lengths increase and as we move towards fixed length packets and fixed routing trajectories it makes more sense to hardware switch and less sense to software switch.

This goes against the present trend in which a number of vendors are promoting general purpose network processors for IP RAN and IP core network applications (including Node B and RNC routers). The selling point of these network processors is that they offer considerable flexibility (which we are saying will not be needed). We also have to consider that this flexibility has a cost in terms of additional processor, memory and bus bandwidth overhead.

Apart from cost implications, these overheads imply higher power consumption and some performance cost in terms of additional end to end delay and delay variability.

One option is to introduce hardware co-processors to speed up time sensitive tasks. but this can result in quite complex (and difficult to manage) hardware/software configuration.

In this month's HOT TOPIC we set out to quantify some of the 'hidden costs' of using generic network processors in 3G network design.

### Packet Arrival Rates

First, we need to decide how much time we have to process a packet. A 40 byte packet has an arrival rate of 160 nanoseconds at OC48 (2.5 Gbps), 35 nanoseconds at OC192 (10 Gbps) and 8 nanoseconds at OC768 (40 Gbps). When you consider that memory access even in high performance S-RAM is around 6 nanoseconds then you can see that you don't have much chance for multiple memory searches at higher throughput rates.

Consider also that classification software can take several hundred clock cycles and a router update can typically take well over 100 cycles. If you want line rate or near line rate processing you would end up with some interesting clock speeds!

### Multi-Layer Classification

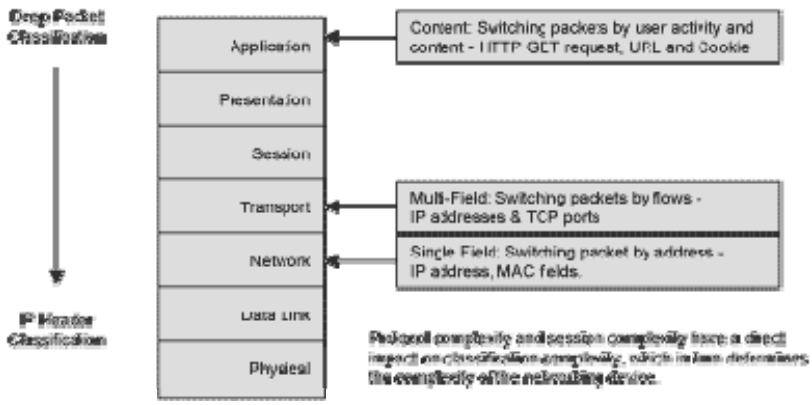


**Figure 1: Multi-layer Classification**

We also need to consider the level of classification used on the packet. If this includes deep packet classification then a data payload search is needed. The data may be several hundred bits long and may be located at random within the payload.

As we move down the protocol stack we find we may have to 'parse' out MPLS headers (4 bytes) or RSVP/Diffserv in addition to the 20 byte IPv4 or 40 byte IPv6 header.

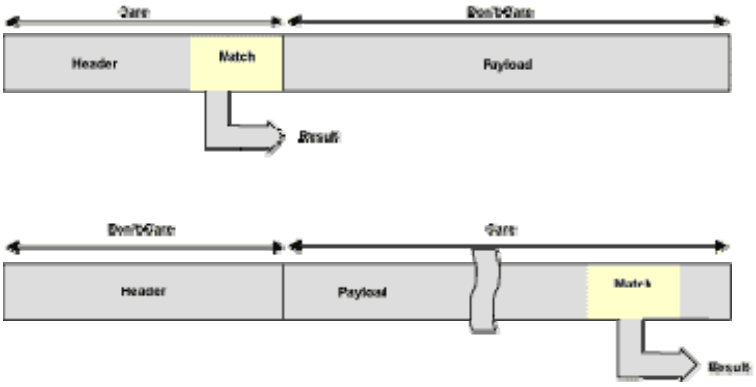


**Figure 2: Header versus data payload searches**

Figure 2 shows that reading a header is relatively straight forward and deterministic but becomes much harder if we need to look into the payload, ie we introduce delay and delay variability into the classification process.

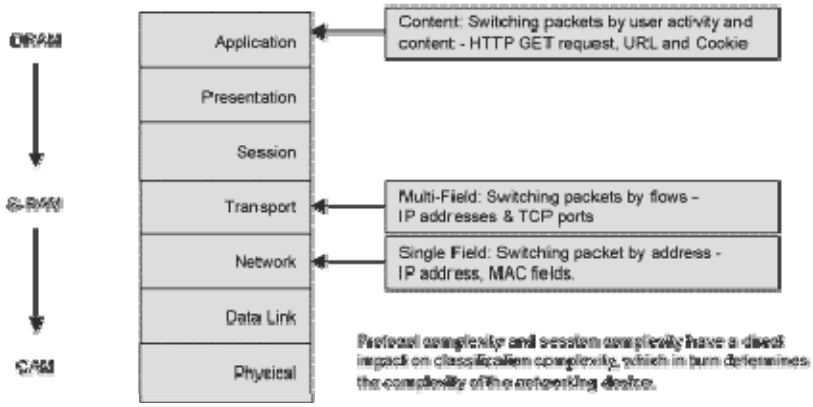


**Figure 3: Classification memory overheads**

The whole process of classification means we have to put the packet somewhere while we examine it. As we move down the protocol stack we need better and better performance from our memory and we can find we end up spending large sums of money, particularly when provisioning S-RAM and CAM (Content addressable memory). Note that these memory overheads are in addition to the buffer memory needed for queue management (prior to accessing egress bandwidth from the router).

Note also that both classification and queue memory need to be substantially over-provisioned to deal with asynchronous and (at times) highly asymmetric traffic.

## The End Result

The end result is that router hardware and router software will cost more than expected and perform less well than expected. In practice, it is probable that acceptable cost and performance will only be achievable from specialised ASICs - we cannot afford the dollar cost, real estate and performance overheads implicit in delivering flexible software/hardware solutions.

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geoff@rttonline.com

00 44 208 744 3163